I. Objection To The Description of the Drawings

In the Office Action, the Examiner objected to the description of Figures 10, 12, 14, 19, 23, 24, and 25, as this description did not mention that each of these drawings appears on two separate sheets. In this Amendment, applicants have amended the Brief Description of the drawings to state that each of these drawings appears on two separate sheets. For instance, the brief description of Figure 10 now states: "Figure 10, which is presented on two separate sheets labeled Figure 10A and 10B, ..." The descriptions of Figures 12, 14, 19, 23, 24, and 25 include similar annotations. Applicants respectfully request reconsideration and withdrawal of the objection to the description of the drawings.

II. Rejection of the Claims Under 35 U.S.C. § 102

The Examiner also rejected claims 1, 2, 14-23, 31-36, 41-45, 48, 49, 52-57 as being anticipated under 35 U.S.C. § 102 by USP 5,973,376 issued to Rostoker et al (Rostoker). In this Amendment, Applicants have canceled claims 1-3, 14-42, and 65-87.

Applicants have re-written claim 4 into an independent claim with all the limitations of canceled claim 1, on which claim 4 originally depended. Applicants note that the Examiner deemed claims 4-13 allowable in the Office Action. Applicants further note that the Examiner also deemed claims 58-64 allowable in the Office Action. Accordingly, Applicants request allowance of these claims at the earliest possible date.

Applicants respectfully traverse the Examiner's rejection of claims 43-45, 48, 49, and 52-57. The Examiner rejected claims 43-45, 48, 49, and 52-57 as being anticipated by Rostoker. Applicants respectfully submit that Rostoker does not anticipate any of these claims. These claims recite a method that places circuit modules by constructing a connection graph with at least one edge that is at least partially diagonal. Rostoker does not disclose, teach, or even suggest such a method. To clarify this distinction further, Applicants have amended the body of

independent claim 43, on which rejected claims 44, 45, 48, 49, and 52-57 depend, to recite "identifying a placement metric based on the connection graph" with the at least one edge that is at least partially diagonal. In view of this amendment and the foregoing remarks, Applicants respectfully request reconsideration and withdrawal of the § 102 rejection of claims 43-45, 48, 49, and 52-57.

CONCLUSION

In view of the foregoing, it is submitted that the currently pending claims, namely claims 3-13, 43-64, and 88-96, are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

Dated: 3/6/03

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AMENDED PARAGRAPHS FOR REPLACEMENT IN THE SPECIFICATION

The following pages provide the amended paragraphs for the specification with the amendments marked with deleted material in [brackets] and new material underlined to show the changes made.

--**Figure 10**, which is presented on two separate sheets labeled **Figure 10A** and **10B**, illustrates a process for generating a wirelength estimate according to a bounding-box method of the invention.--

Please replace the paragraph on page 11, lines 8-9 in the specification with the following amended paragraph.

--**Figure 12**, which is presented on two separate sheets labeled **Figure 12A** and **12B**, illustrates a process for generating a wirelength estimate by constructing MST's that include horizontal, vertical, and 45° edges.--

Please replace the paragraph on page 11, lines 12-13 in the specification with the following amended paragraph.

--**Figure 14**, which is presented on two separate sheets labeled **Figure 14A** and **14B**, illustrates a process for generating a wirelength estimate by constructing Steiner trees with 45° diagonal edges.--

Please replace the paragraph on page 12, lines 3-4 in the specification with the following amended paragraph.

--**Figure 19**, which is presented on two separate sheets labeled **Figure 19A** and **19B**, illustrates a process that generates a congestion cost estimate, and partitions a set of nets, about a cut line.--

Please replace the paragraph on page 12, line 6 in the specification with the following

amended paragraph.

--**Figure 23**, which is presented on two separate sheets labeled **Figure 23A** and **23B**, illustrates one example of a local optimization process.--

Please replace the paragraph on page 12, line 7 in the specification with the following amended paragraph.

--**Figure 24**, which is presented on two separate sheets labeled **Figure 24A** and **24B**, illustrates one example of a simulated annealing process.--

Please replace the paragraph on page 12, line 8 in the specification with the following amended paragraph.

--**Figure 25**, which is presented on two separate sheets labeled **Figure 25A** and **25B**, illustrates one example of a KLFM process.—

THE AMENDED CLAIMS

The following pages provide the amended claims with the amendments marked with deleted material in [brackets] and new material underlined to show the changes made.

4. [The method of claim 1, wherein the IC layout has a number of circuit elements, a net having a set of circuit elements,] For an electronic design automation application, a method of placing circuit modules in an integrated circuit ("IC") layout, wherein the IC layout has a number of circuit elements, a net having a set of circuit elements, the method comprising:

using a diagonal line to measure a placement metric;

wherein using the diagonal line to measure a placement metric comprises calculating an estimate of the length of interconnect lines necessary to connect the circuit elements of said net, wherein the calculation measures the length of at least one line that is at least partially diagonal.

43. For an electronic design automation application, a method of placing circuit modules in an integrated circuit ("IC") layout, wherein said IC layout includes a net and a plurality of circuit elements, wherein the net represents interconnections between a set of circuit elements, the method comprising:

constructing a connection graph that models the topology of interconnect lines for connecting the circuit elements of the net, said connection graph having edges, each edge connecting two circuit elements of the net, wherein at least one of the edges is at least partially diagonal;

identifying a placement metric based on the connection graph.